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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,716	11/18/2003	Anthony Mark Jones	DB000929-001	4927

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,716	JONES, ANTHONY MARK	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 7* is/are rejected.

7)☒ Claim(s) *2-5,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/715,716 filed on 11/18/2003. Claims 1-9 remain pending in the application. This application is a division of 10/124,021, which was subjected to restriction/election, and also filed under Rule 1.47, where the petition was granted (Copy of Petition Decision filed on 11/18/03). Therefore double patenting rejection cannot be applied.

Claim Objections

2. Claim 4 is objected to because of the following informalities: relationship "t $\ll\!\!\ll$" should be changed to --t >> τ-- (See Fig. 12) in order to accurately define the claimed limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al., "A New Gate Delay Model for Simultaneous Switching and Its Applications*," DAC 2001, June 18-22, 2001, ACM 1-58113-297-2/01/0006, pp. 289-294.

5. As to claim 1, Chen et al. teach a method for characterizing a timing delay curve of a circuit component (circuit Fig. 1, where the circuit drives a capacitance load or corner capacitance), said timing delay curve (Fig. 2, 5, 9, 10, 11, 12) having a first region (region to the left of transition point) and a second region (region to the right of transition point) comprising determining a first delay equation representing said first region of the delay curve (general forms of delay equations have been developed, delay equation representing the left region of the transition point Fig. 2, 5, 9, page 294); determining a second delay equation representing said second region of the delay curve (general forms of delay equations have been developed, delay equation representing the right region of the transition point Fig. 2, 5, 9, page 294); and determining a corner capacitance of said circuit component, said corner capacitance representing a transition point from said first region to said second region (Fig. 2, 5, 9, 10, 11, 12; Chen et al. suggest how to perform ITR on our new delay model by identifying worst corners (corner capacitance) used in ITR (page 292); the delay model can be used as the timing model for STA and ITR where the worst case corners need to bed identified; for a model to be used in our method to find the worst case corners, a sufficient condition is that all timing functions of this model are monotonic or bi-tonic respect to each input variable (page 293); we have developed a new model to capture the delay of simultaneous to controlling transitions and input positions; general forms of delay equations have developed; through worst case corners identification, we guarantee the correct propagation of min-max timing ranges for this delay model (page 294).

6. As to claims 6-7, Chen et al. teach determining a first delay equation by determining equation for a curvilinear region of the delay curve and determining a second delay equation by determining a delay equation for a linear region of the delay curve (Fig. 2, 5, 9, 10, 11, 12; a first region, a region to the left of transition point appears to be curvilinear; and a second region, region to the right of transition point appears to be linear).

7. Claims 1 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al., "Efficient Generation of Delay Change Curves for Noise-Aware Static Timing Analysis," IEEE, March, 2002, pp. 1-7.

8. As to claim 1, Agarwal et al. teach a method for characterizing a timing delay curve of a circuit component (Fig. 3, 5, 9, 10, see whole document) comprising determining a first delay equation representing said first region of the delay curve (Fig. 3, 5, 9, 10; delay change curve); determining a second delay equation representing said second region of the delay curve (Fig. 3, 5, 9, 10, delay change curve); and determining a corner capacitance of said circuit component, said corner capacitance representing a transition point from said first region to said second region (Fig. 3, 5, 9, 10, delay change curve comprising transition points or intermediate region where the delay is dynamically changed).

9. As to claims 6-7, Fig. 3, 5, 9 and 10 show transition points, where the delay is dynamical change in the delay curve and where portions of the delay are curvilinear and linear.

Allowable Subject Matter

10. Claims 2-3, 4-5 and 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, claim 4 should be rewritten to clarify the claimed limitation (see Fig. 12). The prior art does not teach or fairly suggest the claimed limitations as recited in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VUTHE SIEK
PRIMARY EXAMINER